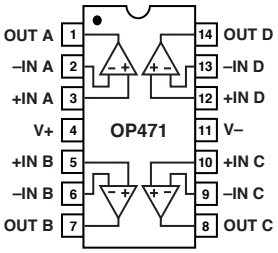
High Speed, Low Noise Quad Operational Amplifier

OP471

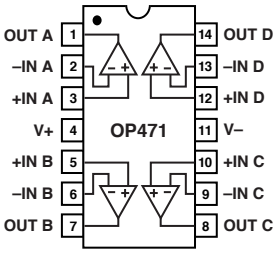
FEATURES
Excellent Speed: 8 V/μs Typ
Low Noise: 11 nV/√Hz @ 1 kHz Max
Unity-Gain Stable
High Gain Bandwidth: 6.5 MHz Typ
Low Input Offset Voltage: 0.8 mV Max
Low Offset Voltage Drift: 4 μV/°C Max
High Gain: 500 V/mV Min
Outstanding CMR: 105 dB Min
Industry Standard Quad Pinouts

PIN CONFIGURATIONS

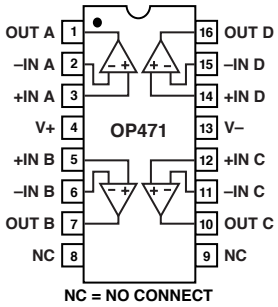
14-Lead Hermetic Dip (Y-Suffix)



14-Lead Plastic Dip (P-Suffix)



16-Lead SOIC (S-Suffix)



GENERAL DESCRIPTION

The OP471 is a monolithic quad op amp featuring low noise, 11 nV/√Hz Max @ 1 kHz, excellent speed, 8 V/μs typical, a gain bandwidth of 6.5 MHz, and unity-gain stability.

The OP471 has an input offset voltage under 0.8 mV and an input offset voltage drift below 4 μV/°C, guaranteed over the full military temperature range. Open-loop gain of the OP471 is over 500,000 into a 10 kΩ load ensuring outstanding gain accuracy and linearity. The input bias current is under 25 nA limiting errors due to signal source resistance. The OP471's CMR of over 105 dB and PSRR of under 5.6 μV/V significantly reduce errors caused by ground noise and power supply fluctuations.

The OP471 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low-noise instrumentation amplifiers, quad buffers and low-noise active filters.

The OP471 conforms to the industry standard 14-lead DIP pinout. It is pin-compatible with the LM148/LM149, HA4741, RM4156, MC33074, TL084 and TL074 quad op amps and can be used to upgrade systems using these devices.

For applications requiring even lower voltage noise the OP470 with a voltage density of 5 nV/√Hz Max @ 1 kHz is recommended.

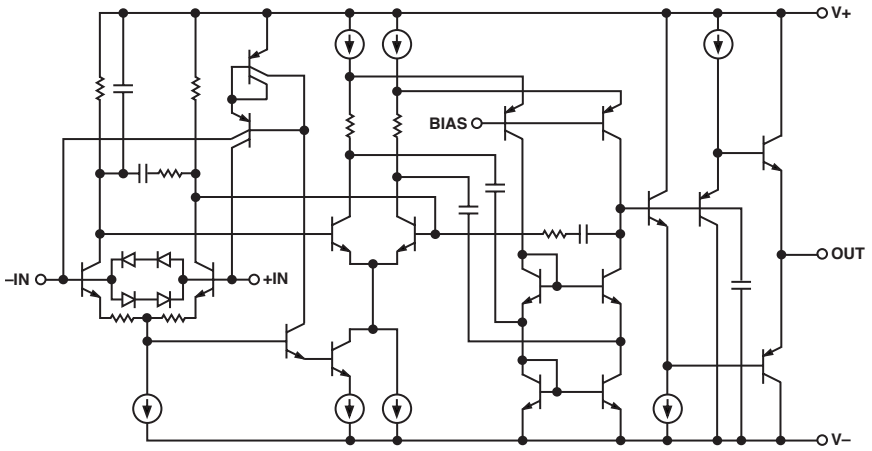


Figure 1. Simplified Schematic

OP471–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP471E Min	OP471E Typ	OP471E Max	OP471F Min	OP471F Typ	OP471F Max	OP471G Min	OP471G Typ	OP471G Max	Unit
Input Offset Voltage	V_{OS}			0.25	0.8		0.5	1.5		1.0	1.8	mV
Input Offset Current	I_{OS}	V_{CM} = 0 V		4	10		7	20		12	30	nA
Input Bias Current	I_B	V_{CM} = 0 V		7	25		15	50		25	60	nA
Input Noise Voltage[1]	e_n p-p	0.1 Hz to 10 Hz		250	500		250	500		250	500	nV p–p
Input Noise Voltage Density[2]	e_n	f_O = 10 Hz f_O = 100 Hz f_O = 1 kHz		9 7 6.5	16 12 11		9 7 6.5	16 12 11		9 7 6.5	16 12 11	nV/√Hz nV/√Hz nV/√Hz
Input Noise Current Density	i_n	f_O = 10 Hz f_O = 100 Hz f_O = 1 kHz		1.7 0.7 0.4			1.7 0.7 0.4			1.7 0 7 0.4		pA√Hz pA√Hz pA√Hz
Large-Signal Voltage Gain	A_{VO}	V = ±10 V R_L = 10 kΩ R_L = 2 kΩ	 500 350	 700 550		 300 175	 500 275		 300 175	 500 275		 V/mV V/mV
Input Voltage Range[3]	IVR		±11	±12		±11	±12		±11	±12		V
Output Voltage Swing	V_O	$R_L \geq$ 2 kΩ	±12	±13		±12	±13		±12	±13		V
Common-Mode Rejection	CMR	V_{CM} = ±11 V	105	120		95	115		95	115		dB
Power Supply Rejection Ratio	PSRR	V_S = 4.5 V to 18 V		1	5.6		5.6	17.8		5.6	17.8	µV/V
Slew Rate	SR		6.5	8		6.5	8		6.5	8		V/µs
Supply Current (All Amplifiers)	I_{SY}	No Load		9.2	11		9.2	11		9.2	11	mA
Gain Bandwidth Product	GBW	Av = 10		6.5			6.5			6.5		MHz
Channel Separation[1]	CS	V_O = 20 V p-p f_O = 10 Hz	125	150		125	150		125	150		dB
Input Capacitance	C_{IN}			2.6			2.6			2.6		pF
Input Resistance Differential-Mode	R_{IN}			1.1			1.1			1.1		MΩ
Input Resistance Common-Mode	R_{INCM}			11			11			11		GΩ
Settling Time	t_S	A_V = 1 To 0.1% To 0.01 %	 	 4.5 7.5		 	 4.5 7.5		 	 4.5 7.5		 µs µs

NOTES
[1]Guaranteed but not 100% tested.
[2]Sample tested.
[3]Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, –25°C ≤ T_A ≤ 85°C for OP471E/F, –40°C ≤ T_A ≤ 85° for OP471G, unless otherwise noted.)

Parameter	Symbol	Conditions	OP471E Min	OP471E Typ	OP471E Max	OP471F Min	OP471F Typ	OP471F Max	OP471G Min	OP471G Typ	OP471G Max	Unit
Input Offset Voltage	V_{OS}			0.3	1.1		0.6	2.0		1.2	2.5	mV
Average Input Offset Voltage Drift	TCV_{OS}			1	4		2	7		4		µV/°C
Input Offset Current	los	V_{CM} = 0 V		5	20		8	40		20	50	nA
Input Bias Current	I_B	V_{CM} = 0 V		13	50		25	70		40	75	nA
Large-Signal Voltage Gain	Avo	V_O = ±10 V R_L = 10 kΩ R_L = 2 kΩ	 375 250	 600 400		 200 125	 400 200		 200 125	 400 200		V/mV
Input Voltage Range*	IVR		±11	±12		±11	±12		±11	±12		V
Output Voltage Swing	V_O	R_L ≥ 2 kΩ	±12	±13		±12	±13		±12	±13		V
Common-Mode Rejection	CMR	V_{CM} = ±11 V	100	115		90	110		90	110		dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V		3.2	10		18	31.6		18	31.6	µV/V
Supply Current (All Amplifiers)	I_{SY}	No Load		9.3	11		9.3	11		9.3	11	mA

*Guaranteed by CMR test.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Differential Input Voltage[2] . . . . . ±1.0 V
Differential Input Current[2] . . . . . ±25 mW
Input Voltage . . . . . Supply Voltage
Output Short-Circuit Duration . . . . . Continuous
Storage Temperature Range
P, Y-Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C
Junction Temperature (T_j) . . . . . –65°C to +150°C
Operating Temperature Range
OP471E, OP471F . . . . . –25°C to +85°C
OP471G . . . . . –40°C to +85°C

NOTES
[1]Absolute Maximum Ratings apply to packaged parts, unless otherwise noted.
[2]The OP471's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±1.0 V, the input current should be limited to ±25 mA.

Package Type	θ_{JA}*	θ_{JC}	Unit
14-Lead Hermetic DIP(Y)	94	10	°C/W
14-Lead Plastic DIP(P)	76	33	°C/W
16-Lead SOIC (S)	88	23	°C/W

*θ_{JA} is specified for worst-case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, CERDIP, PDIP packages; θ_{JA} is specified for device soldered to printed circuit board for SO packages.

ORDERING GUIDE

T_A = 25°C V_{OS} MAX (µV)	Package Options		Operating Temperature Range
	14-Lead CERDIP	Plastic	
800	OP471EY		IND
1,500	OP471FY*		IND
1,800		OP471GP	XIND
1,800		OP471GS	XIND

*Not for new design. Obsolete April 2002.

For military processed devices, please refer to the standard microcircuit drawing (SMD) available at
www.dscc.dla.mil/programs/milspec/default.asp
5962-88565022A - OP471ARCMDA
5962-88565023A - OP471ATCMDA
5962-8856502CA - OP471AYMDA

CAUTION

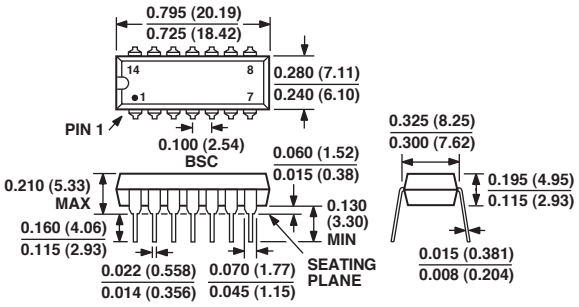
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP471 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

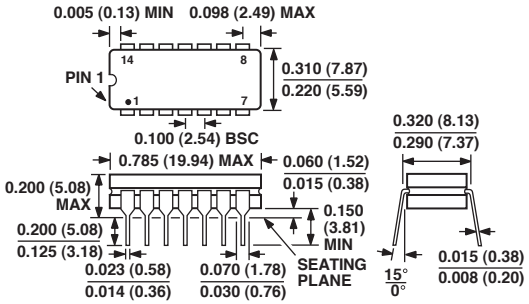
14-Lead PDIP Package

(N-14)



14-Lead CERDIP Package

(Q-14)



16-Lead SOIC Package

(R-16)